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Layout Design of 64 Mb PCRAM Chip Based on 40 nm Process

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Abstract: The layout design based on 40 nm process for the 64Mb phase change random access memory (PCRAM) chip consists of memory cells and peripheral circuits. The chip size is 3 mm×3 mm. 1T1R memory structure with cell size 0.11 μm^2 is used. The sidewall structure is used to minish the size of bottom electrode contact, thus to reduce the operation current and the size of the selector transistor in the memory cell. Dummy for transistor poly-silicon gate is used to reduce the process deviation. Symmetrical wire routings are used to balance the RC delay and guarantee the timing.

Keywords: PCRAM; layout; 1T1R

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Introduction

With the feature size of IC process scaling down to 45nm node and beyond, the mainstream nonvolatile memory FLASH is faced with the fatal limitation of lithography [1]. PCRAM with the significant advantages of good ability to scale down, compatibility with CMOS process, low power, high speed, nonvolatility and high endurance, is considered to be the leading candidate for the next generation of solid state memory [2]. PCRAM is based on chalcogenide material (typically $Ge_2Sb_2Te_5$) with programmable resistance by applying SET and RESET current pulse [3]. The switch between ordered crystalline phase (SET, low resistance) and disordered amorphic phase (RESET, high resistance) can be occurred in a few nanoseconds [4]. Commercial interest is shown among a number of semiconductor manufacturing companies, such as Numonyx, Intel, ST, Samsung, and Hitachi [5-9].

Our SIMIT design team demonstrated an 8 Mb fully functional PCRAM chip based on SMIC 130 nm CMOS process in 2011 [10]. 1T1R memory cell with the size of $50F^2$ is operated by 1.2 V power, while the periphery circuits are supplied by 3.3 V power. The SET current is 0.4 mA, and the RESET current is 2 mA. The bit yield is over 99.9%. The endurance surpass 10^8 times. The chip is successfully demonstrated in a recording system.

In this paper we present a description of the architecture and layout physical design of a 64 Mb fully functional PCRAM chip based on SMIC 40 nm CMOS process. Both array and periphery circuitry are operated under 1.2 V power to minish the whole chip area down to 3 mm×3 mm. Fabrication of the design will be completed in early 2012.

Memory Cell

A vertical cell structure with a NMOS transistor as selector has been introduced to reduce the number of lithographic masks comparing with diode or bipolar selector, thus ensuring lower process cost. The schematic of the 1T1R memory cell is depicted in Fig. 1(a). Here 1.2 V NMOS transistor with gate length 40 nm is used

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to minimize the area occupation. The gate width is limited by the RESET current. The detailed layout of the memory cell with size 0.11 um^2 (20F^2) is shown in Fig. 1(b). The selector NMOS is split into two fingers with shared drain. The vertical bottom electrode contact (BEC) connected to drain is fabricated under metal 1 instead of top metal to reduce dimensions. The sidewall structure is also used to further confine the size of BEC, thus to reduce the RESET current [11].

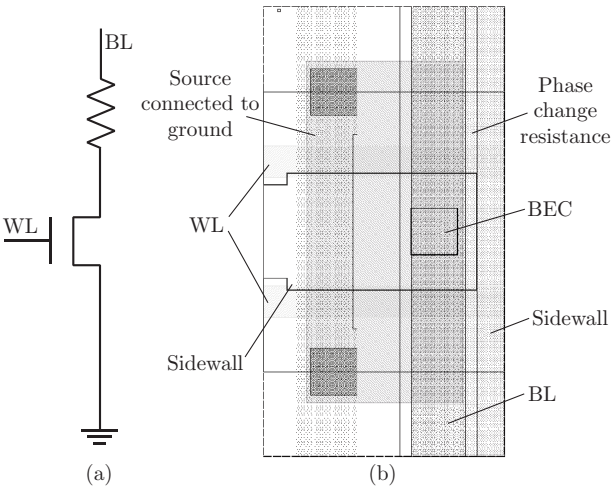

Fig. 1 (a) Schematic of 1T1R memory cellFig, (b). Layout design of 1T1R memory cell.

Chip Architecture

The schematic block diagram of the 64 Mb chip is illustrated in Fig. 2. The memory is organized in four 16 Mb sectors (4096 rows X 4096 columns). Address

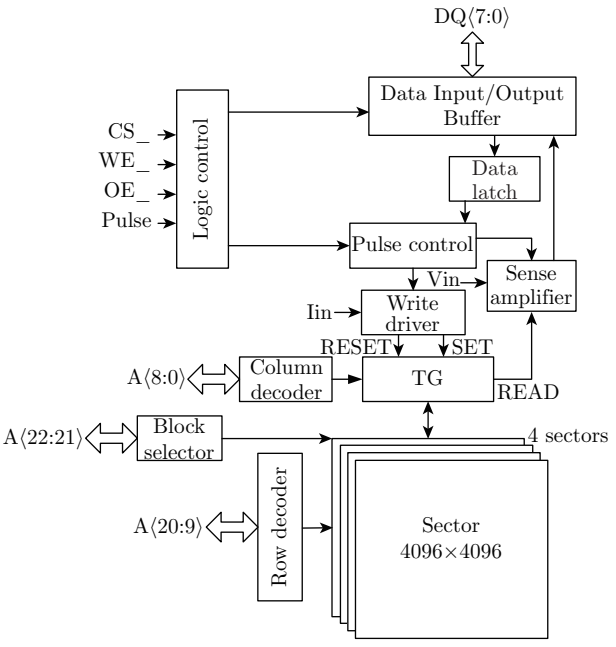

Fig. 2 Chip schematic block diagram.

signals A <22:21> are used to select one of the four sectors. A <20:9> connected to X-Decoder are programmed to select word lines. A <8:0> connected to Y-Decoder are used to enable the transmission gates (TG) which transfer RESET and SET current to 8-parallel bit lines. One Local Sense Amplify is supplied for four bit lines to accelerate the READ speed. Driver circuits feed SET and RESET current to the memory cell. DQ <7:0> are 8-paralle data input/output ports. Latches and Buffers for DQ <7:0> guarantee the validity of the data. Logic control circuits enhance the driver ability of enable signals and sent them to the sectors symmetrically.

Layout Design

The layout architecture of the 64 Mb chip is shown in Fig. 3. The 16 Mb sector is further split into two 8 Mb blocks. Word lines decoded from the X-Decoder and drive by very big buffers are located in the middle of the two blocks. To minish the area occupation, one big buffer is replaced by two much smaller buffers that connected to the left and right block respectively. TG, Y-Decoder and Sense Amplifier (SA) are located in the Y direction. Logic control circuits are placed in the center of the chip in order to balance RC delay of the enable signals sending to the four sectors, hence guarantee the correctness of timing. Latches and Buffers for data I/O are distributed at the edge of the periphery circuitry, near the left and right PAD regions.

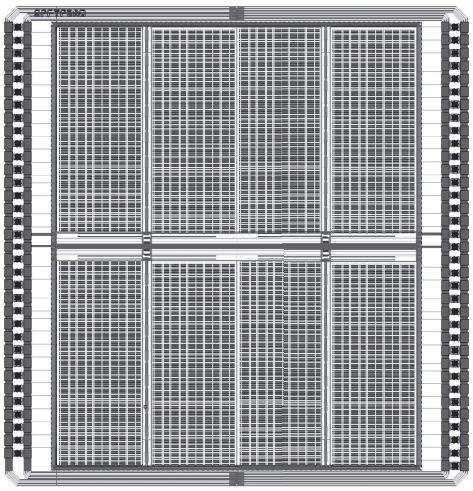

Fig. 3 Chip layout architecture.

To reduce the process deviation, dummies for not only memory array but also TG, Decoder and SA surrounding the real circuits are introduced. Dummy gate for transistor is strong recommended in 40 nm process. Grid of power and ground spread in the whole chip to minimize potential deviation. Power and Ground net for digital circuits and analog circuits are connected to

PAD separately to avoid crosstalk. ESD structures are designed to absorb and dissipate electrostatic discharge energy. The detailed layout design of ESD structure is shown in Fig. 4. Space between drain contacts to poly gate of the ESD transistor is expected to be large enough to minimize the risks of electrostatic discharge. 45° corner of conducting layer in ESD discharge path is required to prevent premature avalanche breakdown. The ESD performance can be improved by removing silicide form the perimeter of the Source and Drain implants in order to provide ballasting to avoid local breakdown. The edge side of ESD devices should be Source rather than Drain to avoid the unwanted parasitic bipolar effect or abnormal discharge path in ESD zapping. The ESD structures located near the respective PADs are necessary to minimize lead resistance and inductances that might otherwise interfere with their operation. Both the power and ground line of ESD structure should be laid as a complete ring and with wide width to ensure the parasitical resistance as low as possible. Guard rings separating the internal region and ESD structures are used to avoid latch up. Antenna effects in big memory array should be estimated and eliminated by adding diode if exist. Chamfer is required at each corner of the chip to reduce local stress.

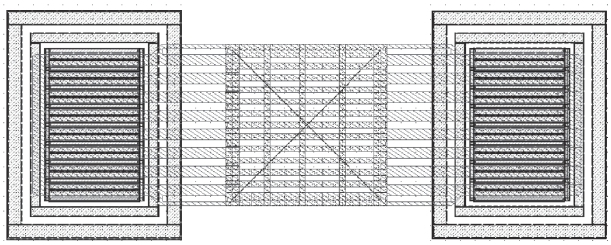

Fig. 4 Layout design of ESD structure.

Summary

A 64 M PCRAM full functional chip using NMOS as cell selector, integrated with 40nm CMOS process, has been presented. The chip architecture and layout design of memory cell have been described in detail. Layout effort in process deviation minimization, power distribution, ESD protection, latch up and antenna prevention has been introduced.

Acknowledgement

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References

[1] G. Atwood, IEEE Trans. Device Mater. Reliab. 4, 301 (2004).

[2] S. J. Hudgens, J. Non-Crys. Solid. 354, 2748 (2008).

[3] S. R. Ovshinsky, Phys. Rev. Lett. 21, 1450 (1968).

[4] W. J. Wang and L. P. Shi, et al. APL 93, 043121 (2008).

[5] C. Villa, et al. ISSCC (2010).

[6] A. Pirovano, et al. Solid-State Electronics 52, 1467 (2008).

[7] R. Annunziata, et al. IEEE (2009).

[8] K. J. Lee, et al. IEEE J. Solid-State Circuits 43, 150 (2008).

[9] Y. Sasago, et al. Symp. VLSI Tech., (2009).

[10] http://www.sh.xinhuanet.com/2011-04/18/content_22549071.htm.

[11] A. Pirovano, et al. IEEE (2003).