Special Issue

http://dx.doi.org/10.3786/sincs2011.09

NANO-MICRO LETTERS ARTICLE

www.nmletters.org

(Proceedings of 2011 Shanghai International Nanotechnology Cooperation Symposium, SINCS 2011, Published online 10 January 2012)

Endurance Analysis of 8M-bits Phase Cha Nge Memory

Linhai Xu*, Xiaogang Chen, Yifeng Chen, Houpeng Chen, Zhitang Song

Abstract: The first Chinese 8M-bits Phase Change Memory (PCM) had been successfully developed basing on the standard 0.13 μm CMOS process. In order to investigate the lifetime of the memory cell, the endurance properties of the memory is analyzed by serials of detailed experiments. The processes of 'stuck-SET' failure and 'stuck-RESET' failure are studied. Meanwhile, with the increasing cycles, an obvious improvement in the RESET/SET window is observed, which induced by SET resistance decrease and RESET resistance increase during the process. Moreover, the RESET and SET resistance distributions changes during the cycling are reported.

Keywords: PCM; endurance; 'stuck- SET' failure; 'stuck-RESET' failure

Citation: Linhai Xu, Xiaogang Chen, Yifeng Chen, Houpeng Chen and Zhitang Song, " Endurance Analysis of 8M-bits Phase Cha Nge Memory", Proceedings of Shanghai International Nanotechnology Cooperation Symposium, 38-41 (2011). http://dx.doi.org/10.3786/sincs2011.09

Introduction

Phase Change Memory (PCM) exploits the large resistance contrast between the crystalline and amorphous phase in chalcogenide material, such as $Ge_2Sb_2Te_5$ (GST) [1]. The crystalline phases (SET state) is characterized by a high optical reflectivity and low electrical resistivity, the amorphous phase (RESET state) has a low optical reflectivity and high electrical resistivity [2]. A high resistance contrast between RESET state and SET state, sometimes up to 3 or 4 orders of magnitude, makes data storage achievable in PCM. Due to the advantages such as non-volatility, high-speed, extended cycling endurance, promising scaling potential and the fine compatibility with the standard CMOS process, PCM has been widely considered as the candidate for the next generation non-volatile memory (NVM).

As for the cycling endurance, it has been reported that PCM device can reach beyond 1E12 RESET/SET cycles [3]. While high-density PCM array experiments in the subsequence show that the endurance numbers are in the range of 1E8-1E10 cycles [4], this result is still much better than the cycling endurance (~1E5) of flash. According to the studies of the cycling endurance, two different failures have been observed, 'stuck-SET' and 'stuck-RESET' failure. In a 'stuck-SET' failure, the device stays in the low resistance and cannot been RESET effectively by the original reset pulse. About the 'stuck-RESET' failure, the device becomes much more resistive than the RESET state and meanwhile cannot be SET into lower resistance through the SET operation pulse. In this paper, we investigate the endurance properties of the first Chinese 8M bits PCM which have been successfully developed using the standard 0.13 μm CMOS process. The resistance properties of the PCM devices during the operational cycles are monitored. Furthermore, the resistance distribution of the array based on single device is also observed.

State Key Laboratory of Functional Materials for Informatics, Laboratory of Nanotechnology, Shanghai Institute of Micro-system and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China
*Corresponding author. E-mail: xulinhai86@mail.sim.ac.cn

Experiments

The transmission electron microscopy (TEM) cross-sectional image of PCM device is showed in Fig. 1(a). The thin GST film is deposited by physical vapor deposition (PVD) method above the heater, which is made of tungsten (W) [5]. By using 0.13 μm standard CMOS process, the diameter of the heater is reduced to generate heat much more effectively at the bottom of the GST film, and as a direct result, the operation current is decreased for low power dissipation.

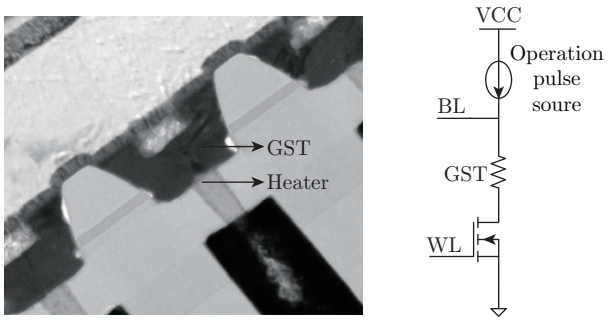

Fig. 1 (a) Transmission equipment electron microscopy (TEM) cross-sectional image of our PCM device, (b) Schematic diagram of our PCM device for testing.

Endurance properties of the device and array are tested with the schematic diagram illustrated in the Fig. 1(b). The operation pulse source is integrated in the current source circuit for operating and reading the device. We choose 1T1R as the memory structure in the 8M-bits PCM. The transistor is used as a selector, which ensures one and only one device is interacting with the operation pulse source on each bitline.

Results and Discussion

In the memory routine tests, we find that the memory has reliable performance with the operation condition as followed: 3.2 mA, 100 ns for RESET and 0.8 mA, 800 ns for SET. With this condition, we perform a serial of experiments to investigate the cycling endurance properties of the memory. The specific results and discussion will be given in the following paragraphs.

The results of the cycling endurance experiments indicate that most of the tested devices can reach beyond 1E7 cycles. A typical 'stuck-RESET' failure is illustrated in Fig. 2. Just as mentioned above, in the 'stuck-RESET' failure, the device resistance enters a state that has a resistance higher than normal RESET

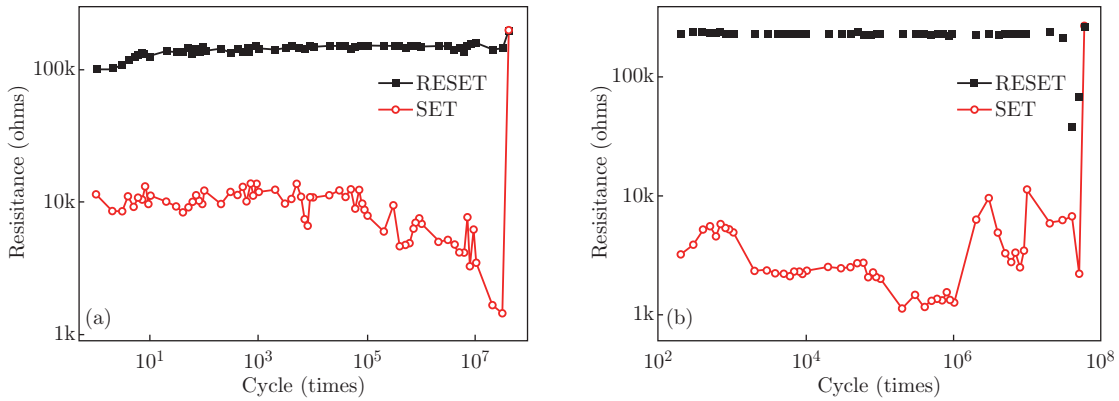

Fig. 2 The typical 'stuck-RESET' failure. (a) The failure occurs suddenly without any indication. (b) The failure occurs after the RESET resistance degrades.

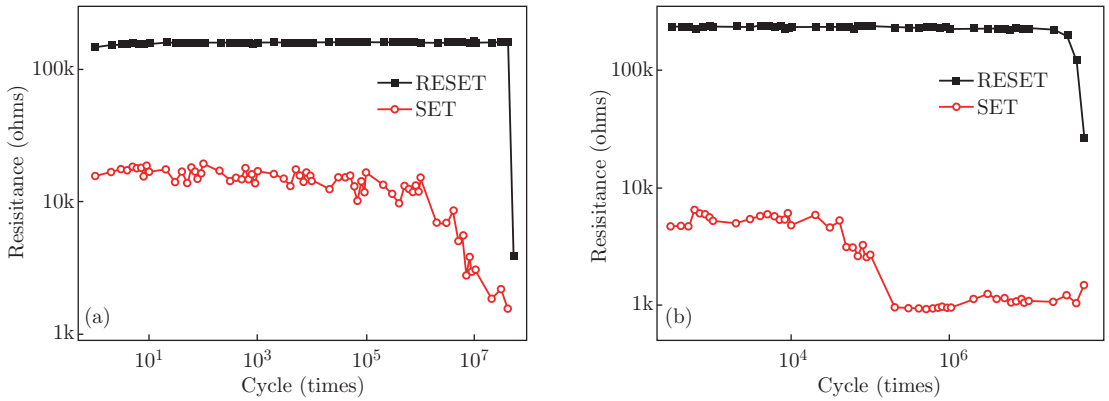

Fig. 3 The representative 'stuck-SET' failure. (a) The failure occurs suddenly. (b) The failure occurs after some degradation in the RESET resistance.

state and lower than the open state. As Fig. 2(a) showed, the device enters the failure suddenly without any indication. The sudden occurrence of the failure makes it difficult to pre-judge the failure is coming. Some other devices present a different behavior as showed in Fig. 2(b), the reset resistance of the device degrades before the failure occurs. The representative 'stuck-SET' failure is show in Fig. 3. As the name described, in the 'stuck-SET' failure, the device can't be RESET anymore even changing the operation condition. The resistance of the device stuck to SET state. Similar to the RESET failure, the 'stuck-SET' failure occurs after some degradation in the RESET resistance or suddenly. Goux et al. [6] have reported that the RESET resistance degradation in the process of 'stuck-SET' failure can be controlled by changing the polarity of the RESET programming pulse, meanwhile, the life time of the memory could be extended to more than 1E10. However, based on the data we get, the 'stuck-SET' failure occurred suddenly wouldn't be recovered by using their method referred. And it is difficult to pre-judge the RESET resistance degradation will lead to which one of the two failures.

It is understood that the two failures have much to do with the stoichiometric change of the phase change material [7]. This study has provided direct evidence show that the atomic composition trends to Antimony (Sb)-rich and Tellurium (Te)-deficient in the active volume (both in crystalline and amorphous phases). And as S.O.Ryu, et al. [8] mentioned, the Sb-rich and Te-deficient is caused by the elements interdiffusion, which are induced by continuous thermal stress during the operation in the system. The segregation of the material elements finally leads into a failure in the device.

As displayed in Fig. 4, a widened RESET/SET window (the resistance difference between RESET and SET) induced by the changes of RESET resistance and SET resistance. The RESET resistance increases and the SET resistance decreases continuously during the programming cycles increase from 1 to 1E7. Switching of RESET resistance and SET resistance can be supposed as a result of the atomic composition variation tendency, which is mentioned above. The biggest change of RESET resistance occurs when the programming cycle is less than 10 times. In comparison, the change of RESET resistance is relatively gentle in the following cycling test. The RESET resistance will be stable until the device reaches the highest that the device can get under the specific test condition. Similarly, if the SET resistance reaches the lowest resistance, it will be stable until one of the failures happens. Moreover, the improvement in the RESET/SET window makes the sensing amplifier read circuit work more effectively and correctly.

In order to comprehensively characterize the changes of RESET resistance and SET resistance, the RESET resistance and SET resistance distributions are investigated in PCM array, as showed in Fig. 5. The tested array is 128 Kb and the programming cycles are 1 and 1E4. The RESET resistance and SET resistance distributions are both approximate log-normal. The SET resistance distribution is improved obviously. At the point of 10Kohm, the cumulative probability increases from 68% of 1 cycle to 85% of 1E4 cycles. Meanwhile, the cumulative probability increase at the top of SET resistance distribution curve improves the array yield. As for the RESET resistance distribution, the lower part has a more obvious improvement, while the higher part holds stable. The statistic results coincide with those obtained through single device. Basing on the statistic results, the performance of the PCM will be improved by applying a number (∼1E4) of RESET/SET operations to the memory before it comes into using, and the endurance properties wouldn't be affected because most of the tested devices show no failure until 1E7 cycles.

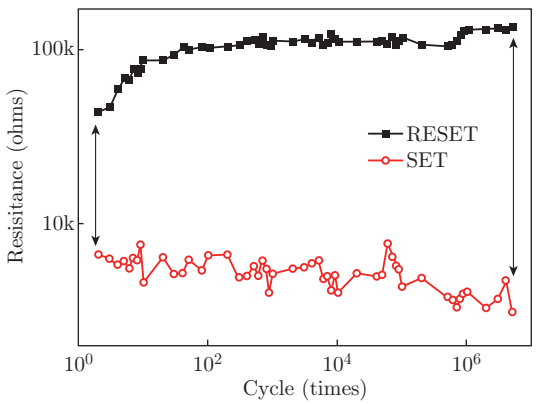

Fig. 4 The changes of RESET resistance and SET resistance lead into a widened RESET/SET window.

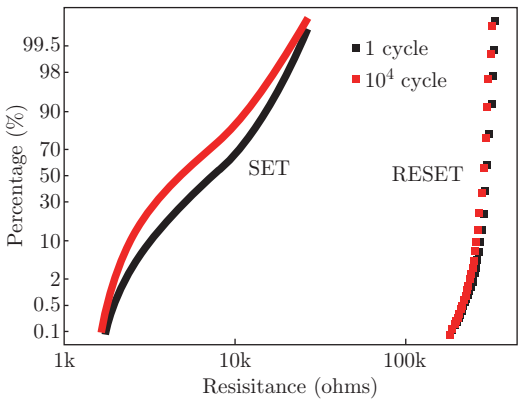

Fig. 5 The RESET resistance and SET resistance distribution changes in PCM array.

Conclusion

In order to research the lifetime of the memory cell, the endurance properties of the memory is studied in detail. The 'stuck-SET' and 'stuck-RESET' failures in PCM both occur after some degradation in the RESET resistance or suddenly without any indication. A widened RESET/SET window results from the continuously increasing RESET resistance and SET resistance. These results are consistent with some known results that the atomic composition phase change material trends to Antimony (Sb)-rich and Tellurium (Te)-deficient during the operation cycles. In addition, we illustrate the RESET and SET resistance distributions changes with cycles, and the statistic results indicate that the performance of the PCM is improved after a number (∼1E4) of RESET/SET operations is applied to the device.

References

[1] G. W. Burr, et al., J.Vacuum Sci. & Tech. B: Microelectronics and Nanometer Structures, vol. 28, 223 (2010).

[2] S. Raoux, et al., IBM J. Research and Development, vol. 52, 465 (2008).

[3] S. Lai and T. Lowrey, in Electron Devices Meeting, 2001. IEDM Technical Digest. International, 36. 5. 1 (2001).

[4] J. Oh, et al., 1 (2006).

[5] Y. F. Chen and et al., Chin. Phys. Lett. vol. 27, 107302 (2010).

[6] L. Goux, et al., Electron Devices, IEEE Trans. on vol. 56, 354 (2009).

[7] J. B. Park, et al., J. The Electrochemical Soc., vol. 154, H139 (2007).

[8] S. O. Ryu, et al., J. The Electrochemical Soc. vol. 153, G234 (2006).